IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. **(Currently Amended)** An input / output signaling apparatus, comprising:

a low voltage input stage that receives low voltage core input signals;

an output stage that provides a higher voltage external output based on the low voltage core input signals; ~~and~~

a cascode stage coupled between the low voltage input stage and the output stage that provides a bias to the output stage and provides a limit for preventing breakdown in the low voltage input stage;

a feedback device coupled to the output stage that prevents static current after a change in value of the external output; and

a keeper device that maintains the changed value of the external output based on operation of the feedback device.

2-3. **(Canceled).**

4. **(Currently amended)** The input / output signaling apparatus of claim 1, wherein a range of the low voltage core input signals is limited to between approximately ~~0 volts~~ 0 volt and 1 volt.

5. (Original) The input / output signaling apparatus of claim 1, wherein a range of the higher voltage external output can exceed a range of the low voltage core input signals by a factor of approximately three.

6. (Original) The input / output signaling apparatus of claim 4, wherein a range of the higher voltage external output can exceed the range of the low voltage core input signals by a factor of approximately three.

7. (Original) The input / output signaling apparatus of claim 6, wherein the range of the higher voltage external output is between approximately 0 volt and 3.3 volts.

8. (Original) The input / output signaling apparatus of claim 1, wherein the low voltage input stage is comprised of a pair of low-voltage transistors having gates respectively coupled to a pair of differential signals corresponding to the low voltage core input signals.

9. (Original) The input / output signaling apparatus of claim 1, wherein the output stage is a current mirror comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

10. (Original) The input / output signaling apparatus of claim 9, wherein the cascode stage is comprised of a pair of transistors having threshold voltages approximately the same as the threshold voltages of the current mirror transistors.

11. (Original) The input / output signaling apparatus of claim 1, wherein the low voltage input stage is comprised of a first pair of low-voltage transistors having gates respectively coupled to a pair of differential signals corresponding to the low voltage core input signals, and

wherein the output stage is a current mirror comprised of a second pair of transistors having threshold voltages in accordance with the higher voltage external output, and

wherein the cascode stage is comprised of a third pair of transistors having threshold voltages approximately the same as the threshold voltages of the current mirror transistors.

12. (Original) The input / output signaling apparatus of claim 7, wherein the low voltage input stage is comprised of a pair of low-voltage transistors having gates respectively coupled to a pair of differential signals corresponding to the low voltage core input signals.

13. (Original) The input / output signaling apparatus of claim 7, wherein the output stage is a current mirror comprised of a pair of transistors having threshold voltages in accordance with the higher voltage external output.

14. (Original) The input / output signaling apparatus of claim 13, wherein the cascode stage is comprised of a pair of transistors having threshold voltages approximately the same as the threshold voltages of the current mirror transistors.

15. (Original) The input / output signaling apparatus of claim 7, wherein the low voltage input stage is comprised of a first pair of low-voltage transistors having gates respectively coupled to a pair of differential signals corresponding to the low voltage core input signals, and

wherein the output stage is a current mirror comprised of a second pair of transistors having threshold voltages in accordance with the higher voltage external output, and

wherein the cascode stage is comprised of a third pair of transistors having threshold voltages approximately the same as the threshold voltages of the current mirror transistors.

16. **(Currently Amended)** An input / output signaling apparatus, comprising:

a low voltage input stage that receives low voltage core input signals;

an output stage that provides a higher voltage external output based on the low voltage core input signals; ~~and~~

a cascode stage coupled between the low voltage input stage and the output stage that provides a bias to the output stage; ~~and~~

a feedback device coupled to the output stage; and

a keeper device that maintains a changed value of the external output based on operation of the feedback device.

17. **(Canceled).**

18. **(Currently amended)** The input / output signaling apparatus of claim 16, wherein a range of the low voltage core input signals is limited to between approximately ~~0 volts~~ 0 volt and 1 volt.

19. (Original) The input / output signaling apparatus of claim 16, wherein a range of the higher voltage external output can exceed a range of the low voltage core input signals by a factor of approximately three.

20. (Original) The input / output signaling apparatus of claim 18, wherein a range of the higher voltage external output can exceed the range of the low voltage core input signals by a factor of approximately three.

21. (Original) The input / output signaling apparatus of claim 20, wherein the range of the higher voltage external output is between approximately 0 volt and 3.3 volts.

22. (Original) The input / output signaling apparatus of claim 16, wherein the bias provided to the output stage provides a limit for preventing breakdown in the low voltage input stage.

23. (Original) The input / output signaling apparatus of claim 16, wherein the feedback device prevents static current after a change in value of the external output.

24. (New) A method for input / output signaling, the method comprising the steps of:

receiving low voltage core input signals;

providing a higher voltage external output based on the low voltage core input signals;

providing a bias to the external output;

providing a feedback signal, the feedback signal relating to a change in value of the external output; and

maintaining the changed value of the external output based the feedback signal.

25. (New) The method of claim 24, wherein a range of the low voltage core input signals is limited to between approximately 0 volt and 1 volt and the range of the higher voltage external output is between approximately 0 volt and 3.3 volts.

26. (New) The method of claim 24, wherein the bias provides a limit for preventing breakdown in the step of receiving the low voltage core input signals.

27. (New) The method of claim 24, wherein the feedback signal prevents static current after the changed value of the external output.